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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,586	FRUTSCHY ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9,65-89 and 91* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3,7-9,65-76,78,79,84,85,89 and 91* is/are allowed.

6)☒ Claim(s) *4-6,77,80-83 and 86-88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04-18-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/18/05 has been entered. An action on the RCE follows.

2. The amendment filed on 4/18/2005 has been entered.

Information Disclosure Statement

3. The Information Disclosure Statement filed on 04-18-05 has been considered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-6, 77, 82, 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. (US Pat. 6452113) in view of Dibene, II et al. (US Pat. 6452804) and Mertol (US Pat. 5898571).

Regarding claim 77, Dibene, II et al. ('113 patent) disclose a power module (see 600 in Fig. 6A/6B) having integrated circuits (IC)/an IC package comprising:

- a substrate (702 of an assembly 700 in Fig. 9 and 7) supporting the microprocessor/IC die (310 in Fig. 7; Col. 8, line 66) on the IC die of the substrate
- the power module (600/602 in Fig. 6A-9) comprising a packaged circuit board (PCB)/package frame (602 in Fig. 6A/6B and 9; Col. 8) mounted/attached at a peripheral area and above a perimeter of the substrate (see Fig. 9 and Fig. 7; Col. 4, lines 25-28; Col. 8, lines 60-68; Col. 9, line 25) and arranged on the die-side of the substrate apart from the IC die on the substrate, and
- the power module providing a low impedance, low inductance power/current path to the die through the circuit components and electrical connectors (see 608A/608B and 612A/612B respectively in Fig. 6A/6B); and being functional as a power/ground impedance deliverer (PGID) to provide power/ground impedance delivery path/circuit (Col. 7, line 53- Col. 9, line 37)

(Fig. 6A-12; Col. 7, line 50- Col 10, line 25).

Dibene, II et al. ('113 patent) further teach:

- the electrical connections/structure providing dual functions including a mechanical and electrical functions where the mechanical function includes the conductive interconnects providing a coupling/rigidity/support for the substrate

(Col. 8, lines 50-60) and mechanical fasteners (802 in Fig. 9) proving the predetermined level of mechanical fastening/stiffening (Col. 9, lines 32-37)

- a variety of module assembly configurations including an embodiment where the package frame (see 2204 in Fig. 22) is positioned/mounted/attached at a peripheral/corner area including a perimeter of the substrate and extends along the perimeter and two side edges of the substrate (see 2204 and 2202 in Fig. 22; Fig. 22-25; Col. 14, line 16- Col. 15, line 22), and
- the substrate being a core substrate having a multiple internal layers in the IC-PCB carrier package (Col. 9, lines 10-30; Col. 7, lines 25-43).

Dibene II, et al. ('113 patent) fail to:

a) explicitly teach the PCB/package frame being a package stiffener, and

b) wherein the stiffener includes a plurality of cooling fins.

a) Dibene, II et al. ('113 patent) further teach another embodiment of Fig. 12, where an entire assembly including the PCB/package frame and a motherboard/stiffener board provides further support and stiffening for the components of the assembly (Col. 10, lines 8-25) such that the PCB/package frame and the motherboard/stiffener board function as the package stiffening components.

Dibene, II et al. ('804 patent) teach an integrated circuit (IC) package having an interposer substrate (104 in Fig. 1) supporting the microprocessor/IC die (101 in Fig. 1)

where a power regulator PCB/electrical conductor assembly (102/103 in Fig. 1) delivering a low inductance current provides a mechanical/fastening support to the interposer substrate through non-compressible mechanical stand-offs/conductors (103 in Fig. 1; Col. 5, line 25; Col. 5, lines 25- 55). An entire assembly of the power regulator PCB/electrical conductor and a motherboard provides further support and stiffening for the components of the assembly such that the power regulator PCB and the motherboard function as the package stiffening components for the three-dimensional Integrated architecture/configuration (Col. 5, line 53- Col. 7, line 25).

b) Dibene II et al. ('113 patent) further teach a heat sink/heat spreader (HS) plate/assembly (1006/1010/1004 in Fig. 10-11B) being integrally bonded to/coupled/supported on the package frame/PGID (Col. 9, line 40-67) such that the package frame/PGID and the IC die are in between the spreader plate and the substrate (see 602, 1006/1004, 302 and 702 respectively in Fig. 6A-11B).

Mertol teaches an IC package having improved heat dissipation wherein a HS structure includes conventional cooling fins (see 100 in Fig. 4-6; Col. 3).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the package stiffener concurrently providing a stiffening support wherein the stiffener includes a plurality of cooling fins as taught by the embodiments in Dibene, II et al. ('113 patent) and Dibene, II et al. ('804 patent) and

Mertol so that the mechanical coupling, thermal performance and the component support can be improved in Dibene, II et al's ('113 patent) package.

Regarding claims 4-6, Dibene II, et al. ('113 and '804 patents) and Mertol teach substantially the entire structure as applied to claim 77 above, wherein Dibene II et al. ('113 patent) teach the substrate being a core substrate having a multiple internal layers in the IC- printed circuit board (IC-PCB) carrier package, the package having a variety of configurations including the flip chip ball grid/array device, built-up multiplayer (BML), pinned grid array- PGA and ceramic land grid array (CLGA), etc. (Col. 9, lines 10-30; Col. 7, lines 25- 43).

Regarding claims 82 and 83, Dibene II, et al. ('113 and '804 patents) and Mertol teach substantially the entire structure as applied to claim 77 above, wherein Dibene II et al. ('113 patent) further teach another embodiment (Fig. 14) where the package frame/PGID comprises rectangular rounded shape with rounded corners (see 1402 and 1404 in Fig. 14; Col. 10, lines 35- Col. 11).

6. Claims 80, 81 and 86-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. ('113 and '804 patents) and Mertol (US Pat. 5898571) as applied to claim 77 above, and further in view of Dehaine et al. (US Pat. 5925925).

Regarding claims 80 and 81, Dibene, II et al. ('113 and '804 patents) and Mertol teach substantially the entire claimed structure as applied to claims 77 above, except the stiffener including at least one of a plurality of power ground sections and a plurality of insulating couplers or a ground path from the die to the substrate.

Dibene, II et al. ('113 patent) further teach the package frame/PGID comprising:

- plated through-holes and electrically conductive surfaces/pads (610, 616A/B respectively in Fig. 6A/B; Col. 8, lines 25-50) being electrically connected to a conductive interconnect spacer having electrically conductive portions (612A/612B in Fig. 6A), the conductive layer/plating being copper (Cu)
- the conductive interconnect spacer providing dual functions including a mechanical support/coupling with the substrate and two separate conductive paths 616A and 616B in Fig. 6A/6B) including a first power path and a second ground path respectively in a coaxial arrangement (Col. 8, lines 50-68), and
- the electrically conductive portions of the conductive interconnect spacer being separated by an insulating dielectric portion/coupling section (612 C in Fig. 6A; Col. 8, lines 37-47).

Dibene, II et al. ('113 patent) further teach in another embodiments of Fig. 13 and 14, the PGID configuration comprising power and ground conductive paths being provided in two concentric metal rings electrically isolated from each other (see

1306/1304 and 1404/1402 respectively in Fig. 13 and 14; Col. 10, lines 35- Col. 11, line 15) and being bonded/soldered to provide an integral structure providing the desired power/ground paths from the die to the substrate.

Dehaine et al. teach a BGA package comprising a frame and a heat dissipating support plate (13 and 17 respectively in Fig. 1 and 3A/3C) where the frame is divided/split into four rings/sections of conductive planes (Q1-Q4 in Fig. 3A/3C) such that each ring/section is separated from each other by an insulating strip/coupling section (23 in Fig. 3A/3C; Col. 10, line 57), such configuration providing a structural integrity for the frame. Furthermore, each ring/section can be electrically connected to different signal potentials/functions such as ground, desired voltage, etc. (see a ground ring 24 in Fig. 3A; Col. 11, line 9) in order to achieve the desired signal transmission and power decoupling functions (Col. 10, line 52- Col. 11, line 18).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the stiffener including at least one of a plurality of power ground sections and a plurality of insulating couplers or a ground path from the die to the substrate as taught by the embodiments of Fig. 13 and 14 in Dibene, II et al. ('113 patent) and Dehaine et al. so that the desired ground/voltage routing and mechanical coupling can be achieved and the signal noise/interference can be reduced in Mertol and Dibene, II et al's ('113 and '804 patents) package.

Regarding claims 86-88, Dibene, II et al. ('113 and '804 patents), Mertol and Dehaine et al. teach substantially the entire claimed structure as applied to claims 77, 80 and 81 above.

Allowable Subject Matter

7. Claims 2, 3, 7-9, 65-76, 78, 79, 84, 85, 89 and 91 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have

questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

05-29-05

NITIN PAREKH

PATENT EXAMINER

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